What is claimed is:

1. An array of phase change memory cells, comprising:

a current source for supplying a read electrical current;

a voltage sensor;

a plurality of conductive bit lines each electrically connected to the current source via a first on/off switch;

a plurality of conductive word lines each electrically connected to a voltage source via a second on/off switch and a first resistor, and to the voltage sensor;

a plurality of memory cells, each including:

a first electrode directly electrically connected to one of the bit lines,

a second electrode directly electrically connected to one of the word lines, and

phase change memory material disposed in electrical contact with the first and second electrodes; and

a reference voltage source connected to the voltage sensor.

2. The array of claim 1, wherein the reference voltage source comprises:

a reference memory cell that includes:

a third electrode electrically connected to the current source,

a fourth electrode electrically connected to the voltage source via a second resistor and to the voltage sensor, and

phase change memory material disposed in electrical contact with the third and fourth electrodes; and

a third on/off switch included in the electrical connection between the third electrode and the current source or the electrical connection between the fourth electrode and the second resistor.

3. The array of claim 1, wherein the reference voltage source comprises:

a plurality of reference memory cells, each including:

a third electrode electrically connected to the current source,

a fourth electrode electrically connected to the voltage source via a second resistor and to the voltage sensor,

phase change memory material disposed in electrical contact with the third and fourth electrodes, and

a third on/off switch included in the electrical connection between the third electrode and the current source or the electrical connection between the fourth electrode and the second resistor;

4. The array of claim 3, wherein a resistivity of the phase change memory material of one of the plurality of reference memory cells is different from that of another one of the plurality of reference memory cells.

5. The array of claim 1, wherein the current source further selectively supplies a programming electrical current that is greater than the read electrical current, and is sufficient in amplitude and duration to alter a resistivity of the phase change material of the memory cells when the programming electrical current flows therethrough.

6. The array of claim 5, wherein for each of the memory cells, one of the first and second electrodes has a resistivity that is higher than that of the other of the first and second electrodes so that the programming electrical current flowing therethrough generates heat therein to heat the phase change memory material.

7. The array of claim 5, wherein each of the memory cells further comprises:

insulation material having a hole formed therein;

spacer material disposed in the hole and having a surface that defines an opening having a width that narrows along a depth of the opening, wherein the memory material is disposed in the opening and extends along the spacer material surface, and wherein one of the first and second electrodes is disposed in the opening and on the volume of memory material;

wherein the one of the first and second electrodes and the volume of memory material form an electrical current path that narrows in width as the current path approaches the other of the first and second electrodes, so that the programming electrical current passing through the current path generates heat for heating the memory material.

8. The array of claim 7, wherein for each of the memory cells, an indentation is formed into the other of the first and second electrodes, and a portion of the memory material extends into the indentation.

9. The array of claim 7, wherein for each of the memory cells, the phase change memory material layer merges together to form a column of the phase change memory material disposed directly over the other of the first and second electrodes such that the current path reaches a minimum cross sectional area at the column.

10. An array of phase change memory cells, comprising:

a current source for supplying a read electrical current;

a voltage sensor;

a plurality of conductive bit lines each electrically connected to the current source;

a plurality of conductive word lines each electrically connected to a voltage source via a first resistor, and to the voltage sensor;

a plurality of memory cells, each including:

a first electrode directly electrically connected to one of the bit lines,

a second electrode directly electrically connected to one of the word lines,

phase change memory material disposed in electrical contact with the first and second electrodes, and

a first on/off switch included in the direct electrical connection between the first electrode and the one bit line or the direct electrical connection between the second electrode and the one word line; and

a reference voltage source connected to the voltage sensor.

11. The array of claim 10, wherein the reference voltage source comprises:

a reference memory cell that includes:

a third electrode electrically connected to the current source,

a fourth electrode electrically connected to the voltage source via a second resistor and to the voltage sensor, and

phase change memory material disposed in electrical contact with the third and fourth electrodes; and

a second on/off switch included in the electrical connection between the third electrode and the current source or the electrical connection between the fourth electrode and the second resistor.

12. The array of claim 10, wherein the reference voltage source comprises:

a plurality of reference memory cells, each including:

a third electrode electrically connected to the current source,

a fourth electrode electrically connected to the voltage source via a second resistor and to the voltage sensor, and

phase change memory material disposed in electrical contact with the third and fourth electrodes, and

a second on/off switch included in the electrical connection between the third electrode and the current source or the electrical connection between the fourth electrode and the second resistor;

13. The array of claim 12, wherein a resistivity of the phase change memory material of one of the plurality of reference memory cells is different from that of another one of the plurality of reference memory cells.

14. The array of claim 10, wherein the current source further selectively supplies a programming electrical current that is greater than the read electrical current, and is sufficient in amplitude and duration to alter a resistivity of the phase change material of the memory cells when the programming electrical current flows therethrough.

15. The array of claim 14, wherein for each of the memory cells, one of the first and second electrodes has a resistivity that is higher than that of the other of the first and second electrodes so that the programming electrical current flowing therethrough generates heat therein to heat the phase change memory material.

16. The array of claim 14, wherein each of the memory cells further comprises:

insulation material having a hole formed therein;

spacer material disposed in the hole and having a surface that defines an opening having a width that narrows along a depth of the opening, wherein the memory material is disposed in the opening and extends along the spacer material surface, and wherein one of the first and second electrodes is disposed in the opening and on the volume of memory material;

wherein the one of the first and second electrodes and the volume of memory material form an electrical current path that narrows in width as the current path approaches the other of the first and second electrodes, so that the programming electrical current passing through the current path generates heat for heating the memory material.

17. The array of claim 16, wherein for each of the memory cells, an indentation is formed into the other of the first and second electrodes, and a portion of the memory material extends into the indentation.

18. The array of claim 16, wherein for each of the memory cells, the phase change memory material layer merges together to form a column of the phase change memory material disposed directly over the other of the first and second electrodes such that the current path reaches a minimum cross sectional area at the column.

19. A method of operating a memory cell array having a current source for supplying electrical current, a voltage sensor, a plurality of conductive bit lines each electrically connected to the current source via a first on/off switch, a plurality of conductive word lines each electrically connected to a voltage source via a second on/off switch and a first resistor and to the voltage sensor, a reference voltage source, and a plurality of memory cells, wherein each of the memory cells includes a first electrode directly electrically connected to one of the bit lines, a second electrode directly electrically connected to one of the word lines, and a phase change memory material disposed in electrical contact with the first and second electrodes, the method comprising:

selecting one of the memory cells by turning on the first and second on/off switches for the bit and word lines directly electrically connected thereto;

supplying a read electrical current from the current source to the bit line directly electrically connected to the selected memory cell, wherein the read electrical current flows through the selected memory cell and produces a first voltage on the word line directly electrically connected thereto;

supplying a reference voltage from the reference voltage source; and

measuring and comparing the first voltage and the reference voltage using the voltage sensor.

20. The method of claim 19, wherein the reference voltage source includes a reference memory cell that has a third electrode electrically connected to the current source, a fourth electrode electrically connected to the voltage source via a second resistor and to the voltage sensor, and phase change memory material disposed in electrical contact with the third and fourth electrodes, wherein a third on/off switch is included in the electrical

connection between the third electrode and the current source or in the electrical connection between the fourth electrode and the second resistor, the method further comprising:

turning the third switch on; and

supplying an electrical current from the current source to the reference memory cell, wherein the electrical current flows through the reference memory cell to produce the reference voltage on the fourth electrode.

21. The method of claim 19, wherein the reference voltage source includes a plurality of reference memory cells each having a third electrode electrically connected to the current source, a fourth electrode electrically connected to the voltage source via a second resistor and to the voltage sensor, phase change memory material disposed in electrical contact with the third and fourth electrodes, and a third on/off switch included in the electrical connection between the third electrode and the current source or in the electrical connection between the fourth electrode and the second resistor, the method further comprising:

selecting one of the reference memory cells by turning on the third on/off switch electrically connected to the selected reference memory cell;

supplying an electrical current from the current source to the selected reference memory cell, wherein the electrical current flows through the selected reference memory cell to produce the reference voltage on the fourth electrode of the selected reference memory cell.

22. The method of claim 19, further comprising:

supplying a programming electrical current that is greater than the read electrical current from the current source to the bit line directly electrically connected to the selected memory cell, wherein the programming electrical current flows through the selected memory cell with an amplitude and duration sufficient to heat the phase change material of the selected memory cell and alter a resistivity thereof.

23. A method of operating a memory cell array having a current source for supplying electrical current, a voltage sensor, a plurality of conductive bit lines each electrically connected to the current source, a plurality of conductive word lines each electrically connected to a voltage source via a first resistor and to the voltage sensor, a reference voltage source, and a plurality of memory cells, wherein each of the memory cells includes a first electrode directly electrically connected to one of the bit lines, a second electrode directly electrically connected to one of the word lines, a phase change memory material disposed in electrical contact with the first and second electrodes, and a first on/off switch included in the direct electrical connection between the first electrode and the one bit line or the direct electrical connection between the second electrode and the one word line, the method comprising:

selecting one of the memory cells by turning on the first on/off switch for the selected memory cell;

supplying a read electrical current from the current source to the bit line directly electrically connected to the selected memory cell, wherein the read electrical current flows through the selected memory cell and produces a first voltage on the word line directly electrically connected thereto;

supplying a reference voltage from the reference voltage source; and

measuring and comparing the first voltage and the reference voltage using the voltage sensor.

24. The method of claim 23, wherein the reference voltage source includes a reference memory cell that has a third electrode electrically connected to the current source, a fourth electrode electrically connected to the voltage source via a second resistor and to the voltage sensor, and phase change memory material disposed in electrical contact with the third and fourth electrodes, wherein a second on/off switch is included in the electrical connection between the third electrode and the current source or in the electrical connection between the fourth electrode and the second resistor, the method further comprising:

turning the second switch on; and

supplying an electrical current from the current source to the reference memory cell, wherein the electrical current flows through the reference memory cell to produce the reference voltage on the fourth electrode.

25. The method of claim 23, wherein the reference voltage source includes a plurality of reference memory cells each having a third electrode electrically connected to the current source, a fourth electrode electrically connected to the voltage source via a second resistor and to the voltage sensor, phase change memory material disposed in electrical contact with the third and fourth electrodes, and a second on/off switch included in the electrical connection between the third electrode and the current source or in the electrical connection between the fourth electrode and the second resistor, the method further comprising:

selecting one of the reference memory cells by turning on the second on/off switch electrically connected to the selected reference memory cell;

supplying an electrical current from the current source to the selected reference memory cell, wherein the electrical current flows through the selected reference memory cell to produce the reference voltage on the fourth electrode.

26. The method of claim 23, further comprising:

supplying a programming electrical current that is greater than the read electrical current from the current source to the bit line directly electrically connected to the selected memory cell, wherein the programming electrical current flows through the selected memory cell with an amplitude and duration sufficient to heat the phase change material of the selected memory cell and alter a resistivity thereof.